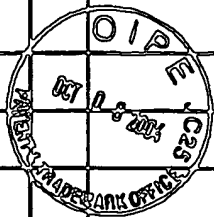


INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional) BUR920040120US1		Application Number 10/711,143
Applicant(s) A. Watson, et al.		
Filing Date August 27, 2004	Group Art Unit 2825	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE



U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
	<i>RE</i>	JP2020039	01/23/1990	Japan		abstract	<input checked="" type="checkbox"/>	

*cont.
11/13/06*

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>RE</i>	SUBSTRATE MODELING AND LUMPED SUBSTRATE RESISTANCE EXTRACTION FOR CMOS ESD/LATCHUP CIRCUIT SIMULATION, T. Li, et al., Coordinated Science Laboratory, Dept. of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, Urbana, IL (1999), 6 pages; 1999 ACM.
<i>RE</i>	BIPOLAR TRANSISTOR ACTION AND TRANSPORT EFFECTS RELATING TO CMOS LATCHUP, G. Krieger, IEEE Transactions on Electron Devices, Vol. ED-34, No. 8, August 1987, pgs. 1719-1728

EXAMINER <i>Phellake Kate</i>	DATE CONSIDERED <i>6/24/06</i>
----------------------------------	-----------------------------------

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.